REMARKS/ARGUMENTS

Claims 6-25 are pending. Claim 6 has been amended. No claim has been added or canceled. No new matter has been added.

In the latest office action, the Examiner rejected claims 6-25 under 35 U.S.C. §103(a) as unpatentable over Hsu (U.S. Patent No. 5,468,981) in view of Gill (U.S. Patent No. 5,418,741) and Stewart (U.S. Patent No. 4,185,319). These claim rejections are overcome as follows.

Embodiments in accordance with the present invention relate to source side programming of EEPROM devices:

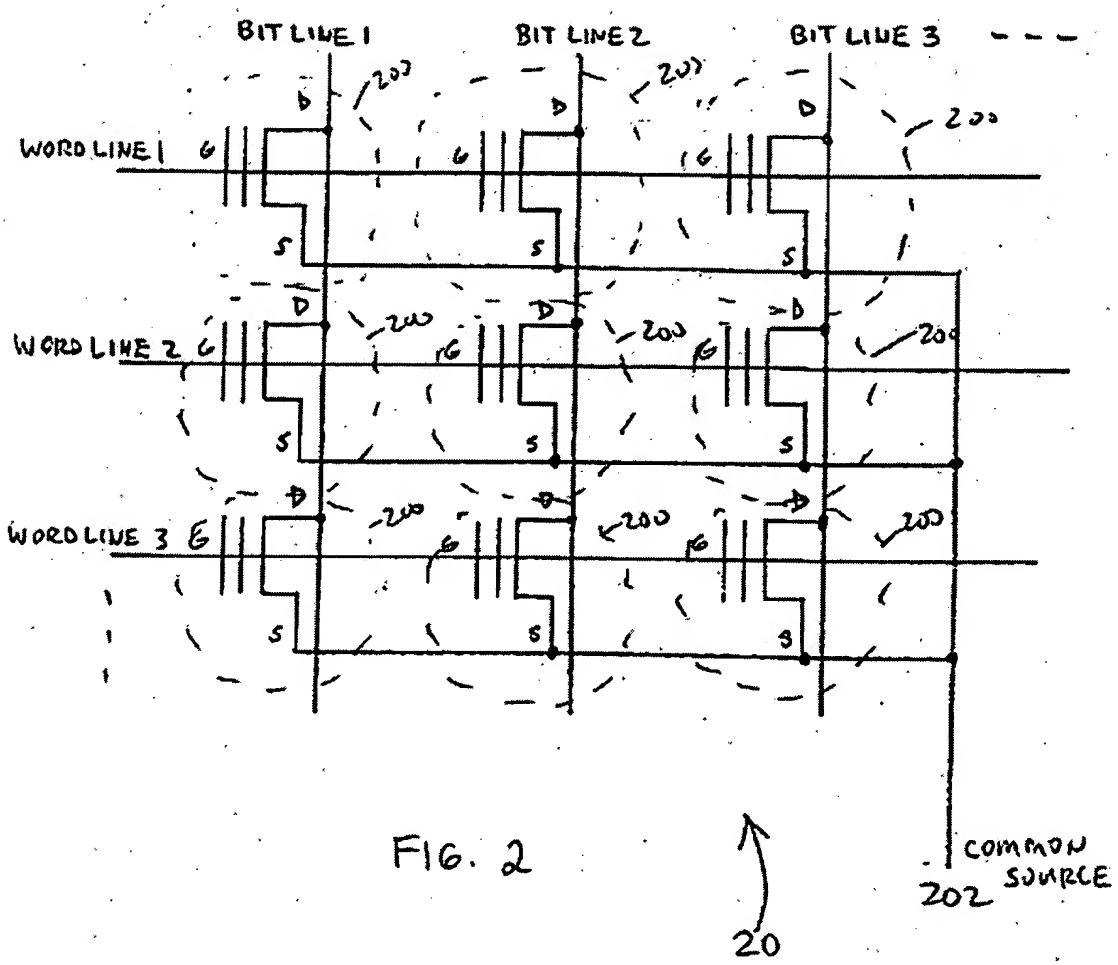


FIG. 2

"A plurality of flash EEPROM cells, similar to the one shown in FIG. 3, can be distributed in a column and row array as in FIG. 2. Whereas drain side programming, as described above in relation of FIGS. 1 and 2, can be performed with this configuration, source side programming of the array can also be performed simply by biasing the common source positive with respect to the drain so that channel hot electrons are generated, flowing in the direction from the selected cell's drain to its source, and tunnel into the floating gate. As described in more detailed below, experimental data of an array having cells similar to the one shown in FIG. 3, reveals that the programming rate is faster for source side programming than it is for drain side programming. An example of bias conditions for a selected cell for source side programming would be, for example, $V_g = 8.5$ volts, $V_d = 0$ volts, $V_s = 4.5$ volts, $V_b = 0$ volts. Non-selected bit lines are left floating (emphasis added, page 6, lines 1-12)."

Pending independent claims 6, 14, and 19 accordingly recite a device in which a source of a memory cell is programmed:

6. A flash memory, comprising:

a plurality of memory cells, each memory cell having a single transistor having a single control gate, a single floating gate, a single drain, and a single source, said plurality of memory cells arranged in an N-row by M-column array, where N and M are integers greater than or equal to one;

N word lines, each word line connecting together the control gates of the transistors in a common and corresponding row;

M bit lines, each bit line connecting together the drains of transistors in a common and corresponding column;

wherein first and second memory cells of the plurality of memory cells are programmed by applying a first voltage to the respective control gates of the first and second memory cells, applying a second voltage to the respective sources of the first and second memory cells and grounding the respective drains of the first and second memory cells,

wherein the sources of the first and second memory cells are coupled to a common node,

wherein the sources of a plurality of memory cells are connected together to a common node. (Emphasis added)

* * *

14. A non-volatile device, comprising:

a substrate;

a floating gate overlying the substrate;

a control gate overlying the floating gate and being electrically coupled to a word line extending in a first direction;

a drain region provided in the substrate and proximate a first end of the floating gate, the drain region extending into the substrate and having a first depth, the drain region having a first graded profile and being electrically coupled to a bit line extending in a second direction that is substantially perpendicular to the first direction; and

a source region provided in the substrate and proximate a second end of the floating gate, the source region and drain region defining a channel therebetween, the source region extending into the substrate and having a second depth that is greater than the first depth, the source region having a second graded profile that is more sloped than the first graded profile,

wherein the control gate is applied with a first voltage and the source region is applied with a second voltage to program the non-volatile device,

wherein the floating gate, control gate, drain region, and source region together define a first memory cell that is configured to store one bit of data,

wherein the non-volatile device further includes a second memory cell that is configured to store one bit of data, the second transistor including a source region that shares a common node with the source region of the first memory cell. (Emphasis added)

* * *

19. A non-volatile semiconductor device, comprising:

a semiconductor substrate; and

a memory cell formed on the substrate, the memory cell including:

a floating gate overlying a surface of the substrate,

a control gate overlying the floating gate and being electrically coupled to a first conductive line extending in a first direction,

a first conductive region provided in the substrate and proximate a first end of the floating gate, the first conductive region extending a first distance into the substrate and having a first graded profile relative to the surface of the substrate, the first conductive region being electrically coupled to a second conductive line extending in a second direction that is substantially perpendicular to the first direction, and

a second conductive region provided in the substrate and proximate a second end of the floating gate, the second conductive region being a double-diffused region that extends a second distance into the substrate and having a second graded profile relative to the surface of the substrate, the second distance being greater than the first distance, the second graded profile having a greater slope relative to the surface of the substrate than the first graded profile,

wherein the control gate is applied with a first voltage and the second conductive region is applied with a second voltage to program the non-volatile device, the second voltage being a positive voltage,

wherein the memory cell is defined by a single transistor. (Emphasis added)

Figures 4 and 5 of the Stewart patent cited by the Examiner are reproduced in part below:

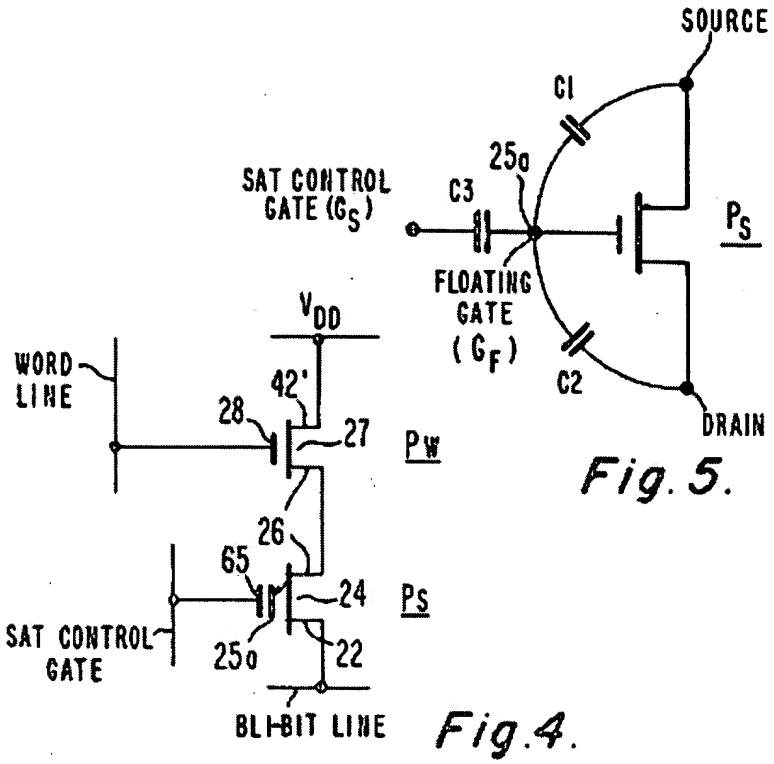


Fig. 5.

Fig. 4.

"To program a floating device P_S an electrical charge must be placed on its floating gate 25a. This is achieved by turning on the P_W transistor whose source drain path is in series with that of the P_S transistor. With reference to FIG. 4, when a potential is applied to word line 28 which is negative with respect to V_{DD} (where V_{DD} is taken way by of example to be 15 volts) P_W is turned on and V_{DD} volts is applied via the conduction path of P_W to region 26 which is the source of P_S. Therefore, to program device P_S, its associated P_W is first turned on by applying an appropriate pulse to the word line and causing V_{DD} volts to be applied to region 26 which functions as the source of P_S. The drain (region 22) of transistor P_S connected to a bit line (e.g., BL_1) is held at a common potential (e.g., ground). A positive potential, for example, 50 volts is applied to the saturation control gate 65. To write the desired information into P_S, the 50 volts applied to its control gate 65, the 15 volts applied to its source, and ground to its drain, must be present for a time of, for example, 10 milliseconds duration (emphasis added, column 4, lines 27-46)."

The Stewart patent discloses using two transistors P_W and P_S to program the device. The use of two transistors to program a cell requires much longer time than using a single cell since the gate of Pw has to be turned on first to apply the necessary voltage to the source of Ps.

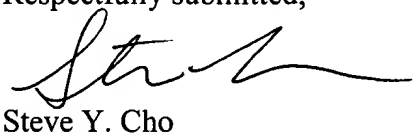
On the other hand, the claimed invention discloses using a single transistor to program each cell. As explained above, one advantage of the present source-side programming is its faster programming speed (e.g., within 10 programming time pulses). This is significantly faster than the conventional drain-side programming, as that disclosed in Hsu. The source side programming, as disclosed in Stewart, results in even slower programming speed than Hsu. Therefore, there is no motivation to combine the two references to arrive at the claimed invention. In fact, Stewart teaches away from the claimed invention since its source-side programming results in slower programming speed, which would discourage the use of source-side programming. Therefore, claims 6, 14, and 19 are allowable.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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